What is claimed is:

1. A method of manufacturing a transistor using a dummy gate pattern, the method comprising:

sequentially depositing on a substrate a first oxide layer, a first nitride layer, a second oxide layer, a second nitride layer;

forming a trench region by etching said second nitride layer, said second oxide layer, said first nitride layer, said first oxide layer and said substrate;

depositing a first insulation layer on said second nitride layer and said trench region;

planarizing said first insulation layer up to said second nitride layer;

forming a dummy gate pattern by etching said second nitride layer, said second oxide layer, said first nitride layer;

forming a lightly doped drain (LDD) underneath both sides of said dummy gate pattern in said substrate and depositing a third nitride layer at both sides of said dummy gate pattern;

removing said second nitride layer;

forming a source and a drain underneath both sides of said dummy gate pattern in said substrate;

depositing a fourth nitride layer and a second insulation layer thereon;

planarizing said second insulation layer up to said fourth nitride layer on said dummy gate pattern;

removing an exposed portion of said fourth nitride layer, said second oxide layer, and said fist nitride layer in said dummy gate pattern;

performing a local channel implantation to form a local channel region in said substrate;

removing said first oxide layer in said dummy gate pattern and growing a third insulation thereto;

forming a gate electrode in said dummy gate pattern.

2. A method as defined by claim 1, further comprising depositing a fourth insulation layer on said gate electrode and said second insulation layer then forming plug after forming said gate electrode.

3. A method as defined by claim 1, wherein planarizing is performed through a chemical mechanical polishing, respectively.

4. A method as defined by claim 1, wherein the second oxide layer is etched away using a wet etching.

5. A method as defined by claim 1, further comprising depositing a fourth insulation layer on said gate electrode and said second insulation layer then forming plug after forming said gate electrode.

6. A method of manufacturing a transistor using a dummy gate pattern, the method comprising:

sequentially depositing on a substrate a first oxide layer, a second oxide layer, a first nitride layer;

forming s trench region by etching said first nitride layer, said second oxide layer, said first oxide layer and said substrate;

depositing a first insulation layer on said first nitride layer and said trench region;

planarizing said first insulation layer up to said first nitride layer;

forming a dummy gate pattern by etching said first nitride, said second oxide layer and said first oxide layer;

forming a lightly doped drain (LDD) underneath both sides of said dummy gate pattern in said substrate and depositing a second nitride layer at both sides of the dummy gate pattern;

forming a source and a drain underneath both sides of said dummy gate pattern in said substrate;

depositing a third nitride layer and a second insulation layer thereon;

planarizing said second insulation layer up to said third nitride layer on said dummy gate pattern;

removing an exposed portion of said third nitride layer, said second oxide layer in said dummy gate pattern;

performing a local channel implantation to form a local channel region in said substrate;

removing said first oxide layer in said dummy gate pattern and growing a third insulation thereto;

forming a gate electrode in the dummy gate pattern.

7. A method as defined by claim 6, wherein planarizing is performed through a chemical mechanical polishing, respectively.

8. A method as defined by claim 6, wherein the second oxide layer is etched away using a wet etching.